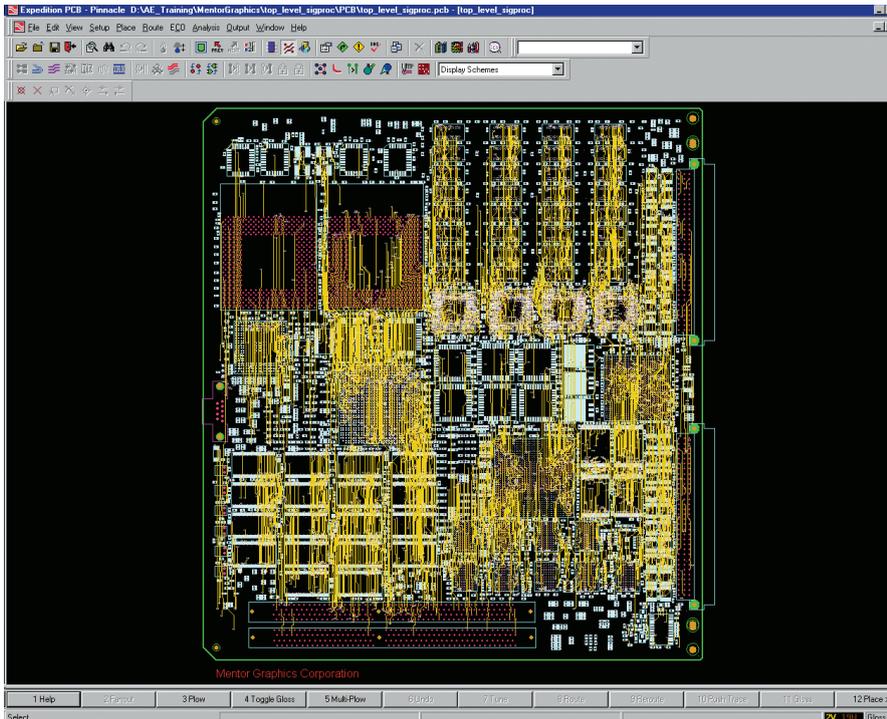


EXPEDITION SERIES

The technology leader for today's most complex PCB systems designs

Mentor
Graphics®





The Expedition Series is simply the most productive solution available for the creation of dense, difficult, high technology PCB designs.

PCB Layout

Expedition PCB, powered by AutoActive technology, is an integral part of the tightly integrated Expedition Series. By combining ease-of-use with advanced functionality, Expedition PCB offers designers the leading technology for the creation of today's most complex designs. Expedition PCB includes interactive and customizable multi-pass autorouting controls for design challenges such as differential pair routing, net tuning, manufacturing optimization and microvia and build-up technology.

AutoActive — The Technology Leader in PCB Design

AutoActive technology represents a revolutionary step forward for PCB design. The power of industry-leading autorouting technology is combined with interactive editing capabilities to produce a single, powerful and easy-to-use design environment. This environment eliminates the burdens of

jumping between tools to get your job done and managing differences between the constraints on the autorouter and on interactive editing.

AutoActive provides designers with greater control than ever before, with the ability to easily switch between automatic and manual editing. From simple tasks, such as defining board areas, to complex procedures that involve maintaining high-speed signal conditions, all objectives are accomplished with the system and the designer working together in real time. The net result of AutoActive technology is reduced design times, increased productivity and unmatched design quality.

What is AutoActive Technology?

- A single, integrated, place and route editing environment that reduces total design time and increases productivity.
- All physical rules and high speed rules are maintained.

- Correct-by-construction design that produces high-quality results with clean-up time eliminated.
- Shape-based, true 45 degree routing.
- The most advanced autorouting technology ever. Stop and start the autorouter at any time and all results will be correct-by-construction.
- Dynamic clean-up of traces through the reduction of segments, prevention of acute angles, and application of pad entry rules.

Dynamic Area Fills

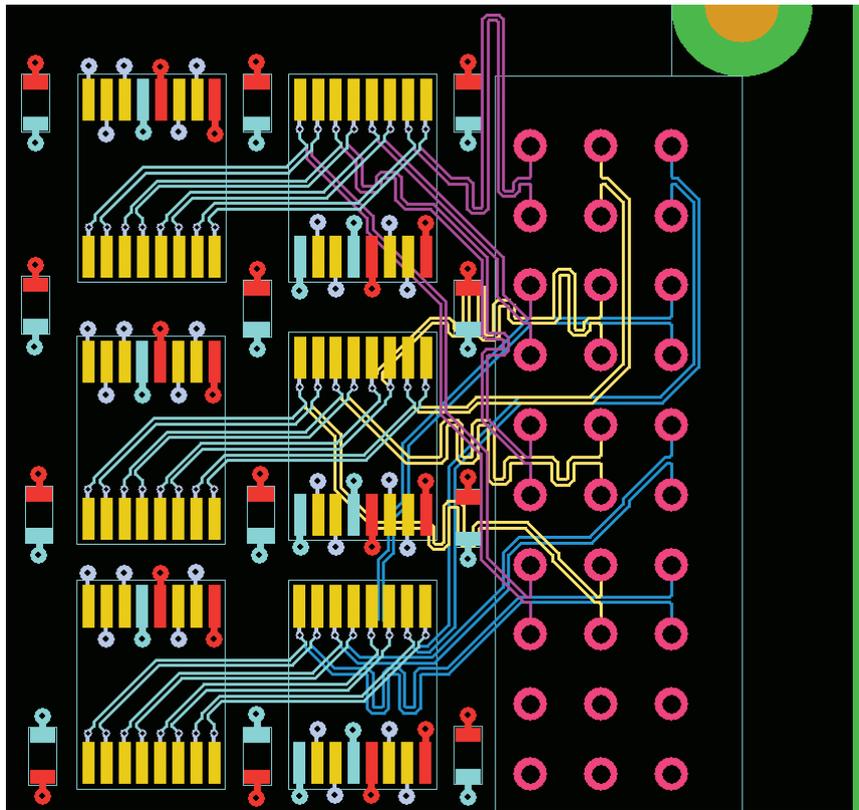
Expedition PCB automatically clears area fills around traces, vias and pads as the board is edited. Dynamic area fills are so fast, Expedition PCB allows you to keep your area fills turned on while you are doing all your edits. Moving a via pushes and shoves other vias, traces and area fills and connectivity is automatically maintained.

Rules By Area

The rules by area functionality greatly improves routing around BGAs and other fine-pitched parts. Rule areas represent complete rule sets that are obeyed by online and batch DRC and in interactive and automatic routing. Rule areas may be defined by layer and can be assigned to any polygon, rectangle or circle. Trace widths and clearances automatically change when traversing into or out of the rule area. You may also change via sizes and spans in a rule area to maximize route completion.

Multiplex With Variable Via Patterns

Expedition PCB's multiplex functionality allows you to simultaneously route multiple nets, including differential pairs, with true 45 degree routing. It can even handle routing through areas of staggered pins. Traces being routed will push and shove the other vias and traces out of the way and automatically clear area fills as needed. Changes can be easily made to a



Routing and editing differential pairs with Expedition PCB is accomplished with speed and ease that will change your view of high-speed design.

variety of selectable via patterns at the touch of a button, allowing enhanced flexibility for routing into dense areas of a design.

Dynamic Hazard Review

Design hazards are dynamically displayed and may be individually selected and colored for easy identification. When a hazard is fixed, it is dynamically removed from the hazard list.

ECOs with Expedition PCB and the Expedition Series

ECOs (engineering change order) can cause delays and introduce errors in the design process. The Expedition Series makes ECOs less painful and more accurate than ever before. Expedition PCB's powerful automation and tight system integration drastically reduces ECO completion times and eliminates synchronization errors.

You can change rules, replace parts and reroute automatically with no rule violations—all in real time.

High-Speed Design with Expedition PCB

Designers today are increasingly challenged by the need to manage signal quality in order to achieve system performance and reduce prototype iterations. High-speed design with Expedition PCB is an integrated part of the AutoActive design environment.

Constraint Definition

Expedition PCB handles an extensive set of constraints to meet high-speed performance requirements whether you're routing interactively or automatically. A common constraint definition environment is shared between schematic capture and layout, allowing the evaluation of critical signals at any

design stage. Constraints include same layer and adjacent layer differential pairs, controlled impedance, net scheduling and delay.

Net Tuning

While routing interactively, graphic tuning aids are displayed for guidance. Nets modified out-of-tune during edits are automatically re-tuned. The Hazards dialog box dynamically updates as you edit nets, providing instant feedback relative to your constraints. Nets can also be tuned automatically within an autoroute pass. Tuned nets are automatically maintained as you complete the design.

Differential Pair Routing

Routing and editing differential pairs with Expedition PCB is accomplished with speed and ease that will change your view of high-speed design. Pair spacing rules can be established by both layer and net class. If one trace in the pair is edited, the other trace in the pair automatically moves with it. Adjacent layer differential pair routing capabilities add another valuable option for routing critical signals on a dense PCB.

Team Design

TeamPCB allows multiple designers to simultaneously work on the same PCB layout design. For PCB designs that are too large or complex to complete in the desired time frame, TeamPCB enables collaboration across geographically dispersed or functionally organized PCB design groups, to maximize productivity and dramatically shorten design times. It is designed for immediate deployment and does not require time-consuming training or changes to a company's infrastructure or library to implement.

Advanced Interconnect Routing

The challenges of advanced interconnect are prevalent today with BGA, CSP, COB and DCA packages increasing board density. Build-up and microvia structures used in these board designs further complicate routing. Expedition PCB, powered by AutoActive technology, offers the leading technology for advanced interconnect designs.

Expedition PCB supports the definition of complex via structure rules and the routing of microvia geometries, including comprehensive via-in-pad rules. Via spans between any two layers are possible. By moving beyond traditional laminate layer pairing, Expedition PCB facilitates the design of build-up structures on laminate to enable escape patterns from dense, high pin count devices. Build-up areas typically have a smaller clearance than the laminate beneath them. Expedition PCB can establish delay values and clearances per via span to address these issues. Additionally, Expedition PCB features true 45 degree routing for BGA fanout and staggered connec-

tors, enabling localized rule definition to facilitate escape paths from dense areas.

Design Reuse

The Design Reuse module creates and stores reusable blocks of circuitry, including schematic and PCB placement and routing data, in a central library. These blocks can then be placed and modified within the same design and across multiple designs. Design reuse automates this process and manages the design data to ensure error free databases and reduce the overall PCB design cycle time.

Variant Management

The Variant Manager tool manages the creation of multiple product configurations from a single design database. Variant Manager's single-point ECO management minimizes errors, reduces costs, improves design quality and enhances production efficiency.

RF Circuit Design with the IFF/Agilent ADS Interface

Many PCB designs, such as cell and handheld phones, incorporate RF circuitry. RF layout design and simulation is a specialized function that is generally carried out in dedicated point tools. With the IFF/Agilent ADS Interface, RF data that is designed, simulated and verified in Agilent's ADS product can be directly imported to and exported from the Design Capture, DesignView and Expedition PCB tools, ensuring that the databases are synchronized and data integrity is maintained.

Setup Parameters

General | Planes | Vias | Layer Stackup | Buried Resistors & Rise Time

Via span definitions and clearances:

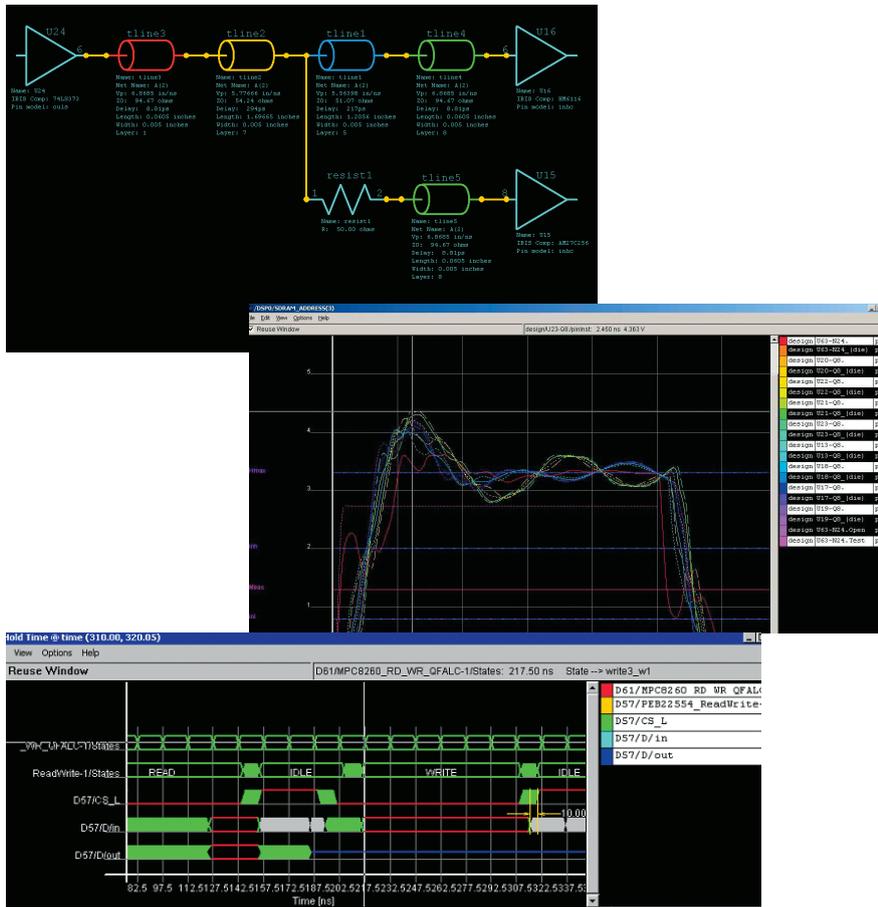
Layer Range	Layer 1-2	Layer 2-3	Layer 3-6	Layer 6-7	Layer 7-8	Through Via
Padstack	L: VIA014BB	L: VIA018BB	L: VIA018BB	L: VIA018BB	L: VIA014BB	L: VIA018
Capacitance (F)	.1p	.1p	.2p	.1p	.1p	.5p
Delay (ns)	.03	.03	.04	.03	.03	.06
Grid (th)	(Default)	(Default)	(Default)	(Default)	(Default)	(Default)

Clearances (th)	Layer 1-2	Layer 2-3	Layer 3-6	Layer 6-7	Layer 7-8	Through Via
<input checked="" type="checkbox"/> General						
Trace-Via	3	5	5	5	3	5
Via-Via 1-2	5	10	[Not Applicable]	[Not Applicable]	[Not Applicable]	10
Via-Via 2-3		5	10	[Not Applicable]	[Not Applicable]	10

Allow stacked vias by using Via Center to Via Center rules when the Same Net Clearances option is selected.

OK Cancel Apply

Expedition PCB offers the leading technology for the creation of advanced interconnect designs.



With Expedition Series, timing and signal integrity issues can be addressed and corrected throughout the design process rather than just at the end.

Signal Integrity and Timing Analysis in the Expedition Series

With the Expedition Series, timing and signal integrity issues can be addressed and corrected throughout the design process rather than just at the end. This ensures that designs are correct the first time, effectively reducing design iterations.

Signal Vision

The Signal Vision tool features a tightly integrated, easy-to-use, what-if environment for exploring signal integrity and timing. It provides a common transmission-line view of a net, whether it is selected in the schematic or in the layout.

ICX™

The Expedition Series leverages the full capabilities of ICX's powerful signal integrity verification functionality. ICX also includes industry-leading simulation model support to increase the accuracy and ease of verification through mixed-signal, multi-lingual, ADMS simulation technology. Rather than going through a traditional design cycle of alternating routing and analysis, ICX's analysis is integrated in real time within the route process, delivering correct-by-construction designs. In addition, routing is accomplished according to electrical constraints to improve design quality, rather than with rules representing converted physical constraints.

Tau®

Tau employs symbolic timing analysis to provide the Expedition Series with the premier solution for the timing verification needs of board-level circuits. Symbolic timing analysis addresses the limitations of traditional static timing tools, such as the identification of a large number of false paths and also eliminates many of the modeling issues found when using static timing tools.

System Verification

Analog Designer will verify analog and mixed analog/digital designs at the system, or board, level. It is tightly integrated into DesignView and combines ease-of-use with powerful simulation, preparation of stimuli, complex analysis of circuits and verification through graphing and output. Analog Designer is PSpice model compliant and provides over 6100 models and analog HDL modeling.

ModelSim® is the world's most popular and widely used VHDL and mixed-VHDL/Verilog simulator and the fastest-growing Verilog simulator. ModelSim products are uniquely architected using technology such as Optimized Direct Compile for faster compile times and simulation performance, Single Kernel Simulation (SKS) and Tcl/Tk for greater levels of openness and faster debugging. Exclusive to ModelSim, these innovations result in leading compiler/simulator performance, complete freedom to mix VHDL and Verilog and the unmatched ability to customize the simulator.

EXPEDITION SERIES DESIGN FLOW

System Design	System Verification	PCB Layout	Fabrication
DesignView	Signal Vision	Expedition PCB	Expedition PCB
Design Capture	Analog Designer	PCB Planner	CAM Output Manager
DxDesigner	BetaSoft Board	PCB Viewer	
FPGA BoardLink	ModelSim	PCB Browser	
Variant Manager	(FPGA Advantage)		
HDL Designer Series (FPGA Advantage)	Tau		
	ICX		
	HyperLynx		

Library Management & Design Data Management

CAM Output Manager

The creation of manufacturing data and the distribution to production sites introduces challenges at a point in the design process where errors can become very costly, in terms of time and dollars. CAM Output Manager provides automated and customizable creation and distribution of manufacturing data that results in increased quality, accuracy and design throughput. The data generation process of CAM Output Manager ensures verified consistency and accuracy and eliminates the potential for costly errors. CAM Output Manager enhances the existing output capabilities of Expedition PCB and supports existing CAM methodologies such as Gerber, ATE and AIS Drill. In addition, CAM Output Manager's variant design support reduces output creation time and increases distribution accuracy.

DMS — Design Data Management

DMS integrates the electronic design process with the supply chain-on the designer's desktop. It ensures complete data consistency, accuracy and availability throughout the design enterprise. Additionally, DMS consolidates multiple data systems, enabling collaboration and life cycle management across multiple vendors, disciplines and sites.

Solutions for New Customers

For new customers, a wide range of services are available to ease the transition to the Expedition Series, including design-ready and high-quality libraries, interfaces to popular front-end tools, design translators and translation services. Whatever your need, Mentor Graphics can help you to get productive quickly.

Support, Education and Consulting

Mentor Graphics offers a full range of services to drive your productivity and success with Expedition Series tools. Customer Support offers award-winning technical assistance, innovative electronic support and high-quality product enhancements. Education Services offers classroom and online training to help you assimilate new tools and technologies into your design environment. Finally, Mentor Consulting is always ready to provide focused expertise in tough design areas.

Hardware Requirements

- Pentium® III or higher
- Memory: 256 MB RAM

OS Requirements

- Windows XP Professional, Windows NT® 4.0 or Windows 2000®



Systems Design Division
Mentor Graphics Corporation
1811 Pike Road
Longmont, CO 80501
720.494.1000 Main
888.482.3322 Sales
www.mentor.com/pcb

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
503.685.7000 Main
800.547.3000 Sales
www.mentor.com

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